CCD Emulator design for LSST Camera

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ABSTRACT

As part of the LSST project, a comprehensive CCD emulator that operates three CCDs simultaneously has been developed for testing multichannel readout electronics. Based on an Altera Cyclone V FPGA for timing and control, the emulator generates 48 channels of simulated video waveform in response to appropriate sequencing of parallel and serial clocks. Two 256Mb serial memory chips are adopted for storage of arbitrary grayscale images. The arbitrary image or fixed pattern image can be generated from the emulator in triple as three real CCDs perform, for qualifying and testing the LSST 3-stripe Science Raft Electronics Board (REB) simultaneously. Using the method of comparator threshold scanning, all 24 parallel clocks and 24 serial clocks from the REB are qualified for sequence, duration and level before the video signal is generated. In addition, 66 channels of input bias and voltages are sampled through the multi-channel ADC to verify that correct values are applied to the CCD.

In addition, either a Gigabit Ethernet connector or USB bus can be used to control and read back from the emulator board. A user-friendly PC software package has been developed for controlling and communicating with the emulator.

Keywords: CCD, Emulator, electronics, LSST

1. INTRODUCTION

A 3.2G pixel wide-field camera consisting of 189 4K x 4K CCDs is under construction within the LSST project[1]. To enable the full 3.2G pixel image to be read out in two seconds, the science focal plane will be highly segmented, with 16 outputs per CCD for a total of 3024 channels[2]. To manage this high-density challenge, custom ASIC-based readout electronics (REB) have been designed, to permit a compact form factor and low power dissipation[3][4].

The complex LSST detector and front-end electronics have required a substantial test development effort, and as part of this effort, a hardware CCD emulator has been designed and fabricated to simulate CCD operation. The emulator generates simulated CCD video output, and also measures and qualifies the bias and clock inputs, validating their levels, timing and sequence. This emulator provides an excellent platform for debugging and testing of the REB, while eliminating the risk of damaging expensive CCD sensors. Automatic software has been developed which can test and qualify REB in less than one minute. This emulator can greatly simplify the testing of the CCD readout electronics and speed up the camera assembly.

Several CCD emulators have been introduced in previous papers[5][6], and the work described in this paper is based on a previous version of this emulator[5]. What distinguishes this work is its ability to process the high density of video channels, which enable this emulator to perform as three 16-channel CCD sensors, and its comprehensive diagnostic features, which can qualify 66 bias and 48 clocks.

2. CONCEPTION

Figure 1 shows the block diagram of the REB test station. The emulator allows three full-frame images (4096 x 4096 pixels/image) to be generated simultaneously, either with fixed pattern images or arbitrary custom images. It has 48 independent video channels that can simulate three 16-channel sensors, e.g. a CCD250(E2V) or a 3800C(ITL). Also, the emulator is capable of qualifying 66-bias and 48-clock signal lines. This multi-channel design gives the emulator a much broader use beyond REB testing. In addition, a heater loop built into the emulator enables the best simulation of the real CCD sensor. Moreover, the Giga-Ethernet and USB ports adopted for this design make the emulator easy to control and access. Both general-purpose and specific REB testing PC software have been developed to control the emulator. Figure 2 shows the emulator board, and the emulator in REB testing.

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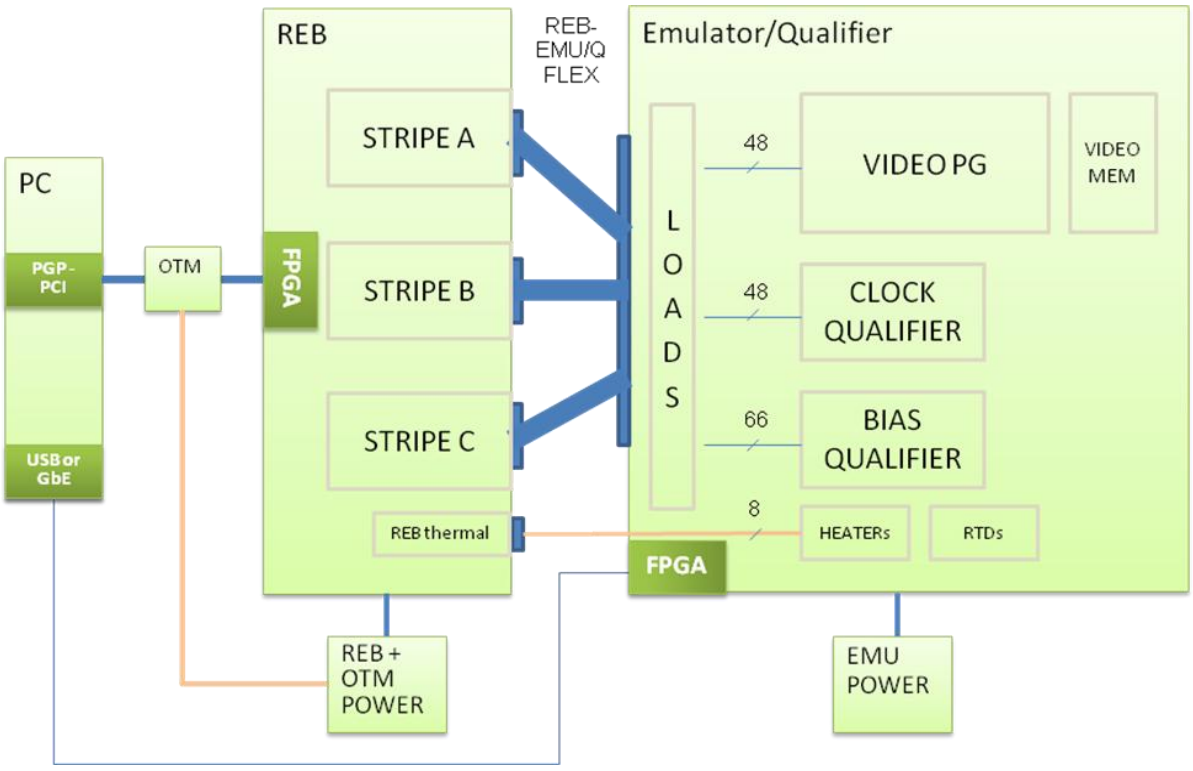
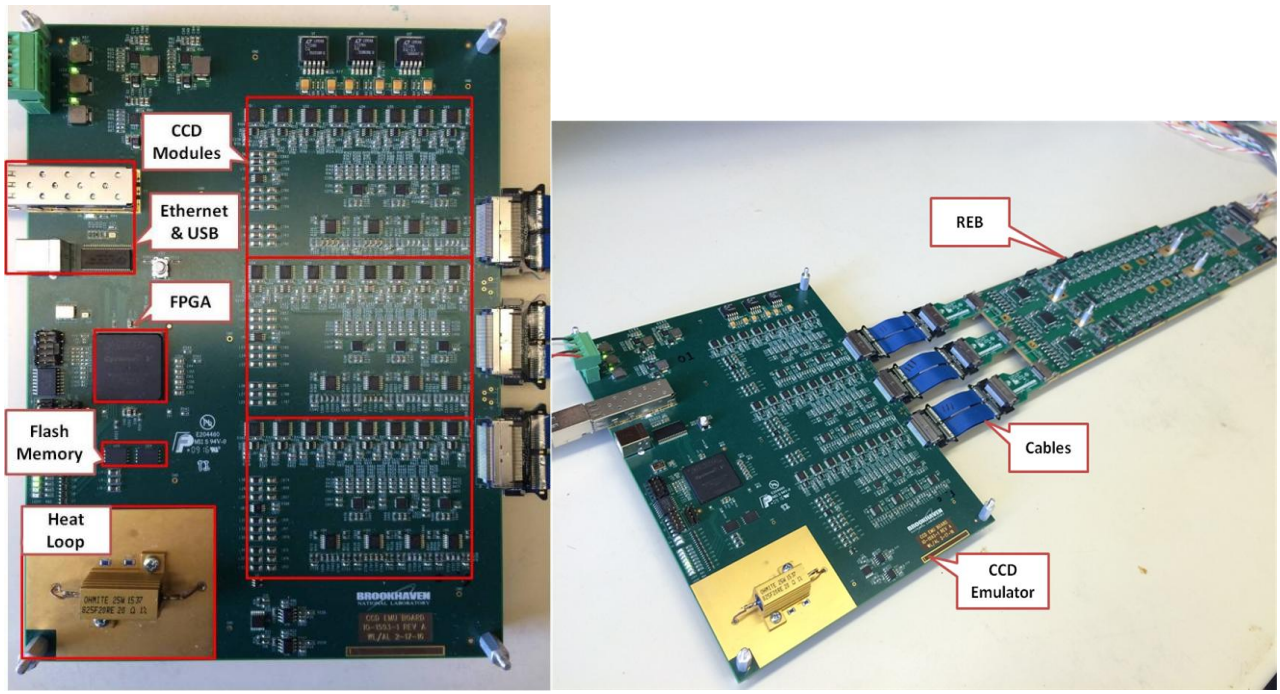


Figure 1, Block diagram of REB test station



(a) (b)

Figure2, (a) CCD Emulator board, (b) Emulator in REB test station

3. ELECTRONICS

The CCD Emulator electronics consist of 5 primary blocks: FPGA, CCD Module, Communicating Ports, Flash Memory and Heater Loop, as shown in Figure 3. The following section will describe each part in detail. The emulator is supplied with +5V, +6V, -6V, and the total power consumption is 4.3W.

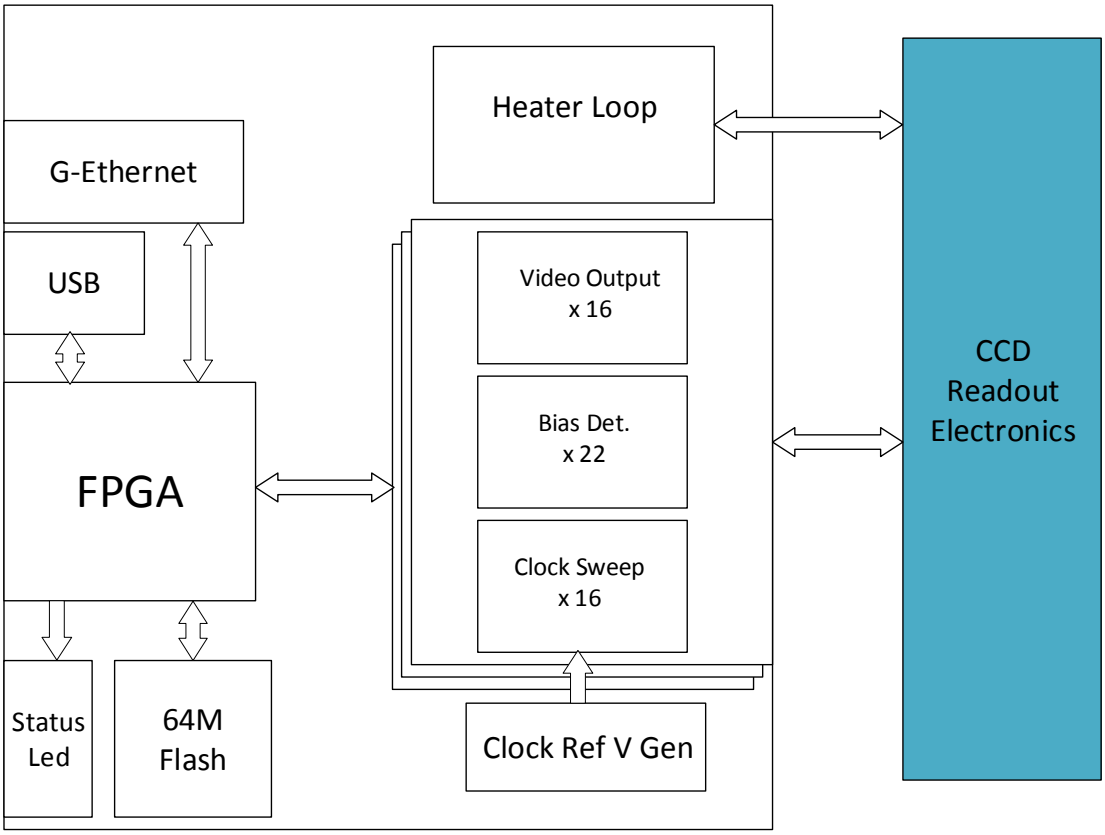


Figure 3. Block diagram of the CCD emulator

3.1 FPGA

An Altera Cyclone V FPGA (5CGXFC7D7F27) is adopted in this design due to the large number of logic elements and user defined IO. The FPGA is the central processor in the design, and all the peripheral blocks are directly connected to it. With specially designed firmware, the FPGA implements the different functions, such as CCD emulation, Clock Sweeping, Bias sampling, USB and Ethernet communication, and Flash memory Read/Write, etc. Even with the multi-channel and multi-function characteristics implemented here, only a fraction of the FPGA resources are used, due to the optimization of the firmware. Table 1 shows the fraction of FPGA resources used. In addition, a 64 Mb PROM (EPCQ64) is connected to the FPGA, for the purpose of power-on configuration.

Table 1. FPGA resources used, in percent.

FPGA Resources	Percent
Logic Elements	10%
Block Memory	4%
PLLs	19%
IO Pins	53%

3.2 CCD Module

Three CCD modules exist in the emulator, and constitute the key part of the emulator. On the one hand, each CCD module works like a real CCD. Once provided with proper bias and clock, it can respond with 16 output video signals. On the other hand, the CCD module checks the bias supplies, and qualifies the clocks in sequence, duration and level. Based on this, the CCD module can be subdivided into 3 parts: Video Generation, Bias Detection, and Clock Detection.

3.2.1 Video Generation

Each CCD module includes 16 channels of output video signal, with a total of 48 channels on the emulator. With many channels for implementation, the diagram was designed as simply as possible. Figure 4(a) shows the diagram for generation of the output video signal, where a 12-bit DAC has been adopted for this design. Due to the high-speed serial interface, the DAC has an update rate of 2.47 MSPS, which is capable of generating the video signal at 1.23 MHz. A high bandwidth amplifier is used for driving the video signal with a rise time of 80 ns when fully loaded. For the best emulation, the CCD output stage is configured with R1 and C1 in the emulator. The drain voltage (OD) generates a current through R1, feeding to the output video signal (OS), while the video signal is transferred out through a block capacitor C1. Figure 4(b) is the actual video signal waveform generated by the emulator.

A video pattern generation algorithm was introduced in a previous version of the emulator[5]. In addition to arbitrary images, several fixed-pattern images can be generated by the emulator, based on the FPGA algorithm. The pattern images include: Flat, Bar (Stripe), Checkerboard, Gradient Horizontal, Gradient Vertical, Pixel-Bar Horizontal, Pixel-Bar Vertical, Pixel Checkerboard, Chirp Horizontal, Chirp Vertical, Chirp Checkerboard, etc.

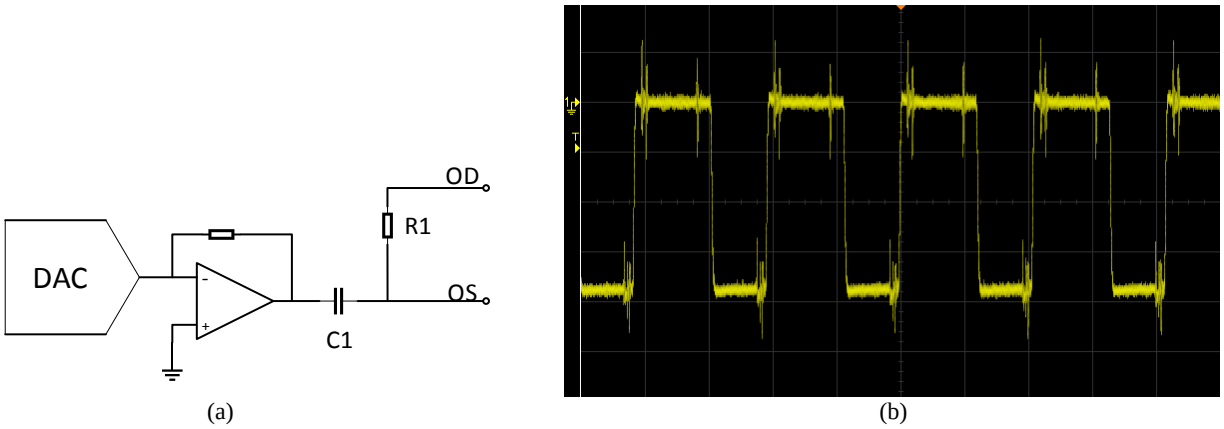


Figure 4. (a)Video generation diagram. (b) Output video signal generated by the CCD emulator.

3.2.2 Bias Detection

Twenty-two bias levels can be qualified in each CCD module, including Output Drain voltage, Reset Drain voltage, Output Gate voltage, etc. Three 8-channel 12-bit ADCs are used to sample these biases. The ADC works at a sampling rate of 1 mega-sample per second (MSa/s).

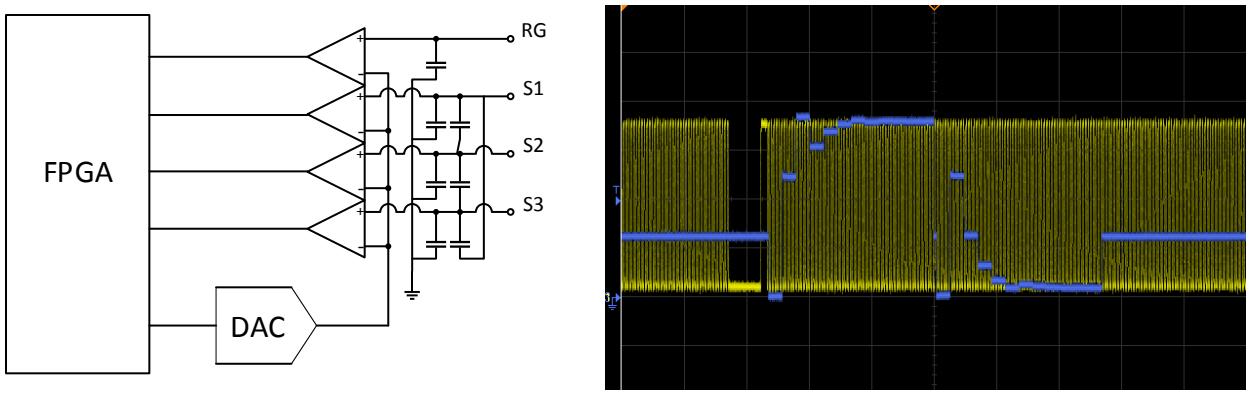
3.2.3 Clock Detection

To meet the LSST REB testing requirements, each CCD module should measure and qualify eight parallel clocks and eight serial clocks. For each clock, all the sequence, duration and level information should be recorded. A special diagram is designed to meet this requirement in a compact schematic architecture.

Figure 5(a) is the diagram of serial clocks and reset gate clock detection. The serial and reset clock are loaded with actual capacitors in much the same way that real CCD sensors have. After the load, the clock is connected to one of the ports of the fast propagation comparator. The other port of the comparator, acting as a threshold of the comparator, is connected with a DAC output, which is controlled by FPGA. The output of the comparator is sampled by the FPGA with a 100 MHz clock. When sweeping the DAC output from low to high, the clock's low and high levels can be determined by counting on the comparator output. The parallel clocks are detected with a similar configuration.

When the emulator is used for qualifying the clock, first the threshold is set at the middle of the clock level. By counting on the output of the comparator, the period of each clock and the sequence of all the clocks can be determined. Second, by sweeping the threshold through the bottom to the top, the low level and high level of each clock can also be determined.

For accuracy, a 12-bit DAC is used to qualify the 10V input signal. All 24 serial clocks share one DAC for the purpose of circuit simplicity. In the sweeping method, a total of 2^{12}=4096 levels should be resolved. As an alternative solution, binary search can also be used to determine clock levels in sequence. Utilizing this method, the total number of levels that should be resolved is: 12 *2*24=576. Compared with the time efficiency, the binary search is applied here. Figure 5(b) shows the binary search process for one serial clock.



(a) (b)

Figure 5. (a) The schematic for Serial clock and Reset Gate clock detection. (b) Clock level sweep in the binary search method. The yellow line is the serial clock signal, while the blue line is the sweeping signal.

3.3 Communicating Ports

Based on FPGA, a self-designed UDP module combines with an Altera Ethernet MAC IP core to implement Giga-Ethernet protocol on the CCD emulator, which is used to communicate with a personal computer. The Ethernet port is mainly used to configure the emulator, to read the testing information from the emulator for offline analysis, and to program the onboard flash memory.

A USB 2.0 port is added as an alternate option for communication. USB 2.0 is implemented with a Cypress CY7C68013A high speed USB peripheral controller.

3.4 Flash Memory

The emulator has two 256 Mb onboard flash memory chips for arbitrary image storage. Each flash memory is capable of storing two 16 M-pixel images. In addition, as high-performance serial flash, each memory has a read/write speed of 416 Mbps, which enable the 16-channel CCD's serial clock to work at as high as 3.25 MHz. Figure 6 shows a 16-channel arbitrary image which was generated by the emulator and read out by the REB.

FPGA firmware has been developed to configure, and to read/write the Flash memory. After power is applied, the configuration module sets the memory into high-speed mode. Through the Ethernet port and flash write module, the PC can write arbitrary image data to the memory. When the CCD emulator works in arbitrary image output mode, the read module delivers memory data to the output video channels.

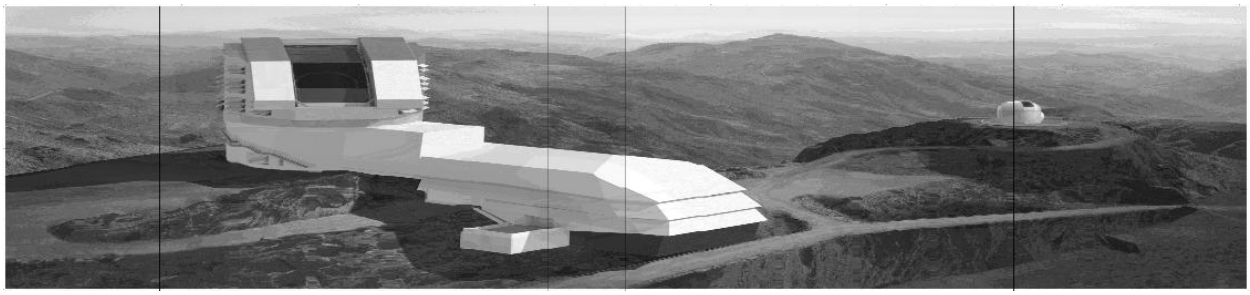


Figure 6. 16-channel arbitrary image generated by CCD emulator.

3.5 Heater Loop

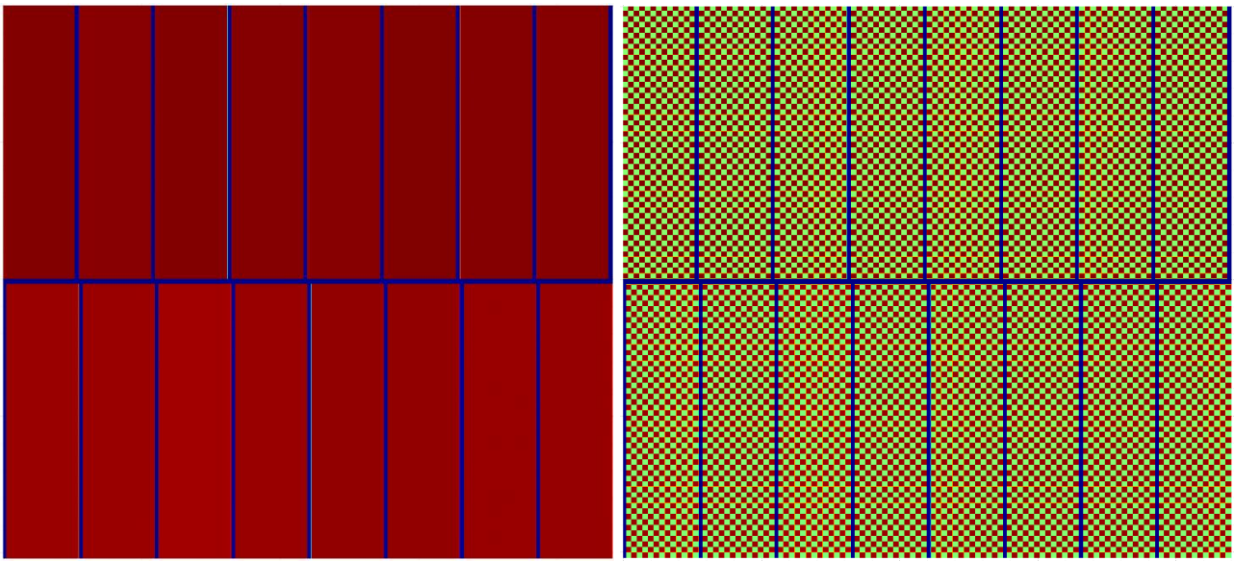
Typically, scientific CCDs use a resistive temperature diode (RTD) sensor to precisely monitor the temperature of the CCD in the cryostat. Normally, there is always a power resistor located at the base-plate of the CCD sensor, to enable the CCD to work at a finely controlled temperature environment by control of the heater loop.

In this CCD emulator, there is one power resistor and four RTD sensors to emulate the heat loop. The heat loop is shown in Figure 2(a) left bottom corner. The specifications of both the power resistor and RTD sensor can be determined by the specific temperature requirement. For the LSST application, a 20 ohm, 25 W power resistor and four 100 ohm RTD sensors are used.

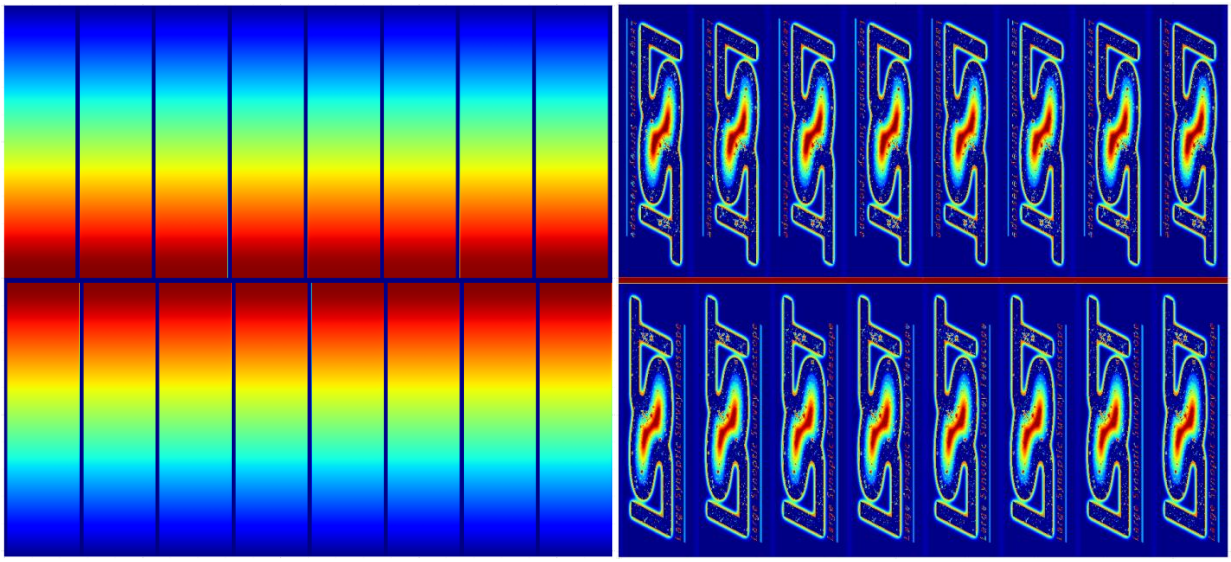
4. TEST

4.1 Video Generation

The pattern image generated by the emulator is useful for qualifying the function and performance of the CCD readout electronics. Several pattern images can be generated by this CCD emulator. Figure 7 shows four full 16-channel CCD pattern images generated by the emulator and read out by the REB.



(a) (b)

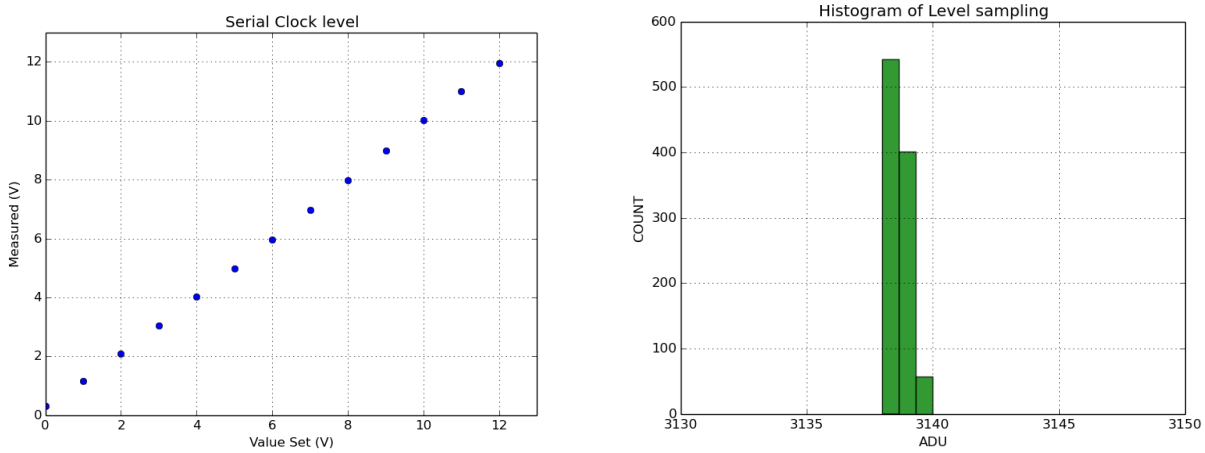


(c) (d)

Figure 7. Video images generated by CCD emulator. (a) Flat Image, (b) Checkerboard, (c) Gradient Vertical, (d) Arbitrary Image (16-channel same).

4.2 Clock Sweep

The resolution of the clock duration is determined by the frequency of the FPGA sampling clock, which is 100 MHz in this design. The linearity and resolution of the clock level sweeping is shown in Figure 8. As in the sweeping DAC, each ADU equals 2.44 mV; the clock sweeping module within this emulator can achieve a resolution of 3 mV.



(a) (b)

Figure 8. Performance of clock level sweeping. (a) Linearity, (b) Histogram.

5. SUMMARY

A high-performance CCD emulator with 48 output video channels, 48 clock detection channels and 66 bias detection channels, has been designed, fabricated and tested. With specially designed cables, the emulator can be used to commission the LSST CCD readout electronics and can speed up the camera assembly. Due to the high performance and multi-channel characteristic, the emulator has potential usage beyond our application as a CCD emulator.

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